were rejected under 35 U.S.C.§102(b) as being anticipated by Watt (U.S. Patent No. 5,745,335). The Applicant respectfully traverses the rejection of these claims, and will demonstrate how the claim language, as amended, distinguishes the instant invention over the cited art in the discussion which follows.

***Farooq et al.*** With respect to claims 1 and 14, element 72 of Farooq et al. is characterized as both a "substrate" and an insulator layer in the Office Action. However, as illustrated in the instant application (Figure 1, elements 202 and 208, respectively), as well as in the Watt reference cited in the Office Action (Figure 1, elements 12 and 14, respectively), the substrate and dielectric are two distinct components which do not contact each other. As is well known to those skilled in the art, and clearly illustrated in Watt, the substrate, dielectric, and conductive layers are typically made of different materials and serve different functions. See Watt, Col. 3, lines 50-58. Thus, simply renaming a dielectric layer (designated as such in Farooq et al.) as a "substrate" does not make it so. Further, *as claimed* by the Applicant, the substrate is not contacted by the first insulating layer. Thus, Farooq et al. does not disclose a substrate, *as claimed* in claims 1, 2, 14-16, and 19 by the Applicant.

Moreover, the Applicant's representative was unable to find any reference whatsoever to "supply voltage interconnect lines", or first and second "integrated circuit die" as asserted in the Office Action with respect to claim 14. Similarly, with respect to claim 16, the term "processor" does not appear to exist anywhere in the Farooq et al. reference, as is asserted in the Office Action. As requested in the prior Response, the Applicant would like some evidence to show that Farooq et al. does indeed disclose these elements *as claimed* by the Applicant.

Finally, with respect to claims 2 and 15, it should be noted that it would be impossible to fabricate C4 lands on the third insulator layer, using the embodiment disclosed by Farooq et al.; since there is no substrate from which to reference the conductive and insulating layers. Further, the C4 lands must contact the "third" conductive layer *as claimed* by the Applicant.

***Naito et al.*** In the Office Action, it is also asserted that Naito et al. discloses a substrate. However, Figure 1 of Naito et al. only recites and illustrates element 32, described as a

"dielectric material layer". Such a continuous dielectric layer is not the same as a substrate, upon which dielectric material and conductive material may be formed, and which does not contact the first insulating layer *as claimed* by the Applicant. Thus, Naito et al. does not disclose a substrate, *as claimed* in claims 1, 8, and 11 by the Applicant.

Further, with respect to claim 8, the same difficulty arises with assigning the designation of a "second conductive layer" to any of the layers illustrated by Naito et al. (as described previously for Farooq et al.). Since there is no substrate shown, there can be no "second" conductive layer.

*Watt* The Office Action asserts that "Watt discloses in Figure 1 a ... substrate (1,2); a first conductive layer 7 located over the substrate ...". However, Watt does not disclose a conductive layer located "over and contacting" a substrate, nor does Watt disclose a first insulating layer contacting the first conductive layer and not contacting the substrate *as claimed* in claims 1, 7, and 9 by the Applicant.

Further, with respect to claim 9, Watt does not disclose a "third plurality of conductive vias" as claimed by the Applicant. Again, as was noted by the Applicant in the previous Response, element reference numbers 38, 40, and 46 do not appear to exist in any of the drawings of Figure 5, as is asserted in the Office Action. The Applicant respectfully requests that the location of these elements in Watt be designated with more precision. Otherwise, it is impossible for the Applicant's representative to provide an adequate response to the concerns expressed by the Examiner.

In summary, since Farooq et al., Naito et al., and Watt fail to disclose each and every element of the invention as claimed by the applicant, especially including a "first conductive layer located over and contacting the substrate", nor a "first insulator layer not contacting the substrate", it is respectfully requested that the rejection of claims 1, 2, 7-9, 11, 14-16, and 19 under § 102 be reconsidered and withdrawn.

Rejections Under 35 U.S.C.§103

Claims 2-3 were rejected under 35 U.S.C.§103(a) as being unpatentable over Naito et al. (EP 0,917,165 A2) in view of Farooq et al. (U.S. Patent No. 6,072,690); claims 4-5, 13, and 21 were rejected under 35 U.S.C.§103(a) as being unpatentable over Naito et al. (EP 0,917,165 A2); claims 6 and 10 were rejected under 35 U.S.C.§103(a) as being unpatentable over Watt (U.S. Patent No. 5,745,335) in view of Yach et al. (U.S. Patent No. 6,225,678); claim 12 was rejected under 35 U.S.C.§103(a) as being unpatentable over Naito et al. (EP 0,917,165 A2) in view of Yach et al. (U.S. Patent No. 6,225,678); claims 18 and 20 were rejected under 35 U.S.C.§103(a) as being unpatentable over Farooq et al. (U.S. Patent No. 6,072,690) in view of Yach et al. (U.S. Patent No. 6,225,678); and claim 17 was rejected under 35 U.S.C.§103(a) as being unpatentable over Farooq et al. (U.S. Patent No. 6,072,690). The Applicant respectfully traverses these rejections of the claims, and will demonstrate how the claim language, as amended, distinguishes the instant invention over the cited art in the discussion which follows.

***Claims 2-3: Naito et al. in view of Farooq et al.*** Neither Naito et al. nor Farooq et al. disclose a substrate, as discussed previously, and claimed by the Applicant. Thus no combination of these references can supply the defective element. Further, even were the defective element to be supplied, the Office Action assertion as to the obviousness of the combination is not supported by the references.

To establish a prima facie case of obviousness, the references themselves must provide a suggestion or motivation for combination. MPEP §2143.01. References must be considered in their entirety, including parts that teach away from the claims. MPEP 2141.02. "Obvious to try" is not a proper standard for determining obviousness. *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir., 1988). "One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed Cir., 1988).

While the purported reason to combine the references in this case is to "prevent the capacitor from collapsing onto the high frequency circuit board during the connection phase", no such problem is recited in either reference. Rather, Naito et al. merely seeks to reduce the ESL

of the capacitor, and Farooq et al. attempts to transfer signals using low-K sheathing around conductors. Thus, no motivation to combine the references is provided.

Further, with respect to claim 2, as noted above, it would be impossible to fabricate C4 lands so as to contact the third insulator layer, *as claimed* by the Applicant, using the embodiment disclosed by Farooq et al. in Figure 3C. Also, since there is no substrate from which to reference the conductive and insulator layers, there can be no "third" conductive layer upon which to fabricate C4 lands.

Finally, the Office Action admits that Naito et al. fails to disclose "C4 lands in electrical contact with the plurality of vias" with respect to claim 2, and then goes on to assert that Naito et al. discloses such lands in Figure 2, with respect to claim 3. This is a direct contradiction, and confusing. Further elaboration is respectfully requested so the Applicant's representative may properly address the Examiner's concerns.

***Claims 4-5, 13, and 21: Naito et al.*** As discussed previously, Naito et al. fails to disclose the element of a substrate, as claimed by the Applicant. It is also admitted that Naito et al. fails to disclose $BaSrTiO_3$ (SBT) as an insulator material, as well as metal conductors made of copper. A multitude of references are cited by the examiner to support the use of SBT in capacitors; however, no reason whatever is given to combine such references with Naito et al. It is merely asserted that SBT is an obvious design choice. However, as noted in Farooq et al., the choice of SBT (a high-K material) is not always appropriate, and is therefore not obvious. See Farooq et al. col. 5, lines 27-32.

Similarly, it is asserted that copper is a "well-known electrode". Again, while a multitude of references are cited, no reason whatever is given to combine the references.

Since no reason has been given to combine the references, and since all of the claimed elements are not found in the Naito et al. reference, the Applicant again respectfully traverses the rejection and requests reconsideration.

***Claims 6 and 10: Watt in view of Yach et al.*** The defects of Watt have been previously discussed, namely, that Watt fails to teach a conductive layer located "over and contacting" a

substrate, *as claimed* by the Applicant. Further, it is not appropriate to combine the Watt and Yach et al. references. As mentioned in the previous Response, Yach et al. is directed toward connecting multiple capacitors to form a matched array. Watt recites only a single capacitor. One of ordinary skill in the art would not be moved to make a "matched array" of capacitors using the mesa-configuration of Watt. In fact, Watt teaches away from such a combination, describing "custom arrays" (i.e. non-matched capacitors), as shown in Figures 5 and 6.

Finally, the assertion in the Office Action that one would likely connect "a plurality of like capacitors together to provide an increased capacitance for an electrical system" is supported by no reference whatsoever. As is well known to those skilled in the art, it is often necessary to connect unlike capacitances together to achieve proper bypass characteristics in electrical circuitry - connecting like capacitances is wasteful and non-productive in such cases. Since no reference is supplied to support this assertion, it appears the Examiner is using personal knowledge, and the Examiner is thus respectfully requested to submit an affidavit is required by 37 C.F.R. § 1.104(d)(2).

***Claim 12: Naito et al. in view of Yach et al.*** The defects of Naito et al. have been previously discussed, namely, that Naito et al. fails to teach a substrate, *as claimed* by the Applicant. Further, it is not appropriate to combine the Naito et al. and Yach et al. references. Yach et al. is directed toward connecting multiple capacitors to form a matched array. Naito et al. recites only a single capacitor. As noted with respect to claims 6 and 10 previously, one of ordinary skill in the art would not be moved to make a "matched array" of capacitors out of the single capacitor which is the subject of Naito et al. Finally, no suggestion to combine the references is provided from the references themselves. Again, it appears the Examiner is using personal knowledge to assert the obviousness of connecting like capacitors in an electrical system, and the Examiner is thus respectfully requested to submit an affidavit is required by 37 C.F.R. § 1.104(d)(2).

***Claims 18 and 20: Farooq et al. in view of Yach et al.*** The defects of Farooq et al. have been previously discussed, namely, that Farooq et al. fails to teach a substrate, *as claimed* by the Applicant. Further, it is not appropriate to combine the Farooq et al. and Yach et al. references.

Yach et al. is directed toward connecting multiple capacitors to form a matched array. Farooq et al. recites only a single capacitor. One of ordinary skill in the art would not be moved to make a "matched array" of capacitors out of the single capacitor which is the subject of Farooq et al. Finally, no suggestion to combine the references is provided from the references themselves. Again, it appears the Examiner is using personal knowledge to assert the obviousness of connecting like capacitors in an electrical system, and the Examiner is thus respectfully requested to submit an affidavit is required by 37 C.F.R. § 1.104(d)(2).

***Claim 17: Farooq et al.*** As discussed previously, Farooq et al. fails to disclose the element of a substrate, as claimed by the Applicant. It is also admitted that Farooq et al. fails to disclose SBT as an insulator material. In fact, Farooq et al. teaches away from the use of SBT as an insulator, since it is noted that a low-K material can be key to the construction of a capacitor. See Farooq et al. col. 5, lines 27-32. As noted in the previous Response, since all of the claimed elements are not found in the reference, the Applicant assumes that the Examiner is taking official notice of the missing elements. The Applicant respectfully objects to such official notice using a single reference obviousness rejection, and pursuant to M.P.E.P. § 2144.03, respectfully traverses the assertion of official notice and respectfully requests that additional references be cited in support of this position.

In summary, since Farooq et al., Naito et al., Watt, and Yach et al. fail to disclose each and every element of the invention as claimed by the applicant, especially including a "first conductive layer located over and contacting the substrate", as well as "first insulator layer not contacting the substrate", and since no motivation to combine the references has been provided, it is respectfully requested that the rejection of claims 2-6, 10, 12, 13, 17, 18, 20, and 21 under § 103 be reconsidered and withdrawn. It should be noted that if an independent claim is nonobvious under 35 U.S.C.§ 103, then any claim depending therefrom is nonobvious. See M.P.E.P. § 2143.03

## Conclusion

Applicant respectfully submits that claims 1-21 are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney Mark Muller at 210/308-5677 or the below signed attorney facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box RCE, Commissioner of Patents, Washington, D.C. 20231, on this 15 day of January, 2002.

Jan e E. Brockschink
Name

Signature

**Clean Version of Pending Claims**

MULTI-LAYER CHIP CAPACITOR
Applicant: Larry Eugene Mosley
Serial No.: 09/537,274

1. (Twice Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductor layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductor layers.

2. (Once Amended) The multi layer integrated circuit capacitor of claim 1 further comprising a plurality of controlled collapse chip connection (C4) lands fabricated on and contacting the third insulator layer and in electrical contact with the plurality of conductive vias.

3. The multi layer integrated circuit capacitor of claim 2 wherein the C4 lands are fabricated in staggered columns in a plan view.

4. The multi layer integrated circuit capacitor of claim 1 wherein at least one of the conductive layers comprise a metal material and at least one of the insulator layers comprise $BaSrTiO_3$.

5. The multi layer integrated circuit capacitor of claim 4 wherein at least one of the conductive layers are fabricated from a copper.

6. The multi layer integrated circuit capacitor of claim 1 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect the plurality of conductive vias.

7. The multi layer integrated circuit capacitor of claim 1 wherein the second and third conductive layers are fabricated in a plurality of strips, such that a surface area of the second conductive layer is less than a surface area of the first conductive layer and a surface area of the third conductive layer is less than the surface area of the second conductive layer.

8. The multi layer integrated circuit capacitor of claim 1 wherein some of the plurality of conductive vias pass through the second conductive layer without forming an electrical connection with the second conductive layer.

9. (Twice Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer, the second conductive layer being fabricated as a plurality of laterally spaced strips such that a surface area of the second conductive layer is less than a surface area of the first conductive layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer, the third conductive layer being fabricated as a plurality of laterally spaced strips such that a surface area of the third conductive layer is less than the surface area of the second conductive layer;

a third insulator layer located over the third conductive layer;

a first plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the third conductive layer;

a second plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the second conductive layer; and

a third plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first conductive layer.

10. The multi layer integrated circuit capacitor of claim 9 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect at least one of the pluralities of conductive vias.

11. (Twice Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer;

a first plurality of conductive vias downwardly extending through the third insulator layer, the third conductive layer, the second insulator layer, the second conductive layer and the

first insulator layer to provide electrical interconnection to the first and third conductive layers; and

a second plurality of conductive vias downwardly extending through the third insulator layer, the third conductive layer, and the second insulator layer to provide electrical interconnection to the second conductive layer.

12. The multi layer integrated circuit capacitor of claim 11 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect at least one of the pluralities of conductive vias.

13. The multi layer integrated circuit capacitor of claim 11 wherein at least one of the conductive layers comprise a metal material and wherein at least one of the insulator layers comprise $BaSrTiO_3$.

14. (Twice Amended) A circuit board assembly comprising:

a circuit board having a pair of supply voltage interconnect lines;

a first integrated circuit die mounted on the circuit board and electrically connected to the supply voltage interconnect lines; and

a second integrated circuit die mounted on the circuit board and electrically connected to the supply voltage interconnect lines, the second integrated circuit die comprising a capacitor having:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers.

15. (Once Amended) The circuit board assembly of claim 14 wherein the second integrated circuit die comprises a plurality of controlled collapse chip connection (C4) lands that are electrically connected to the plurality of conductive vias and the supply voltage interconnect lines.

16. The circuit board assembly of claim 14 wherein the first integrated circuit package is a processor circuit.

17. The circuit board assembly of claim 14 wherein at least one of the conductive layers comprise a metal material and wherein at least one of the insulator layers comprise $BaSrTiO_3$.

18. The circuit board assembly of claim 14 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect the plurality of plurality of conductive vias.

19. (Twice Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second, and third conductive layers, the plurality of conductive vias further extending through the substrate to provide electrical interconnection to both a top surface and a bottom surface of the integrated circuit capacitor.

20. The multi layer integrated circuit capacitor of claim 19 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect the plurality of conductive vias.

21. The multi layer integrated circuit capacitor of claim 1 wherein each of the conductor layers comprise a metal material and wherein each of the insulator layers comprise $BaSrTiO_3$.